REMARKS

This application has been carefully reviewed in light of the Office Action dated April 15, 2010. Claims 1, 3 to 7, 20, 22 to 26 and 39 remain pending in the application, of which Claims 1, 20 and 39 are independent. Reconsideration and further examination are respectfully requested.

Claims 20 and 22 to 26 were rejected under 35 U.S.C. § 101. The rejections are traversed and the Examiner is requested to reconsider and withdraw the rejections in light of the following comments.

The Office Action asserts that applicant has "not provided explicit and deliberate definitions of which particular apparatus/machine is used for executing" each of the claimed steps, and that the method "would be reasonably interpreted as a series of steps completely performed mentally, verbally, or without a machine . . . ." Applicant wholly disagrees with this assertion because those skilled in the art readily understand that each of the claimed steps, when read in light of the specification and drawings, is executed on an image processing apparatus. The specification and drawings specifically describe various computational hardware elements implementing the steps of the method (see, e.g., Figs. 1, 2, 4, 6, 8 and 9 describing bit connecting circuit 1, line buffer 8, diffusion filter 9, etc.), and computer elements on which the claimed steps can be implemented (see, e.g., Fig. 10 where the image processing apparatus is implemented in personal computer 1010 containing a microprocessor (MPU) and memory (ROM)). Further, it is submitted that interpreting the claimed method as a series of steps that could be performed mentally or verbally is simply not reasonable. The sheer number of computations and storage required to perform this method of image processing and quantization precludes the practicality of it

being performed mentally. Those skilled in the art readily understand that each of the claimed steps, when read in light of the specification and drawings, are executed by computational hardware. Thus, the specification describes more than sufficient structure to support each claimed step.

Nonetheless, without conceding the correctness of the rejections, Claim 20 has been amended to make it clearer that the method is one executed in an image processing apparatus and therefore, the claim is believed to be statutory. Accordingly, reconsideration and withdrawal of the § 101 rejections are respectfully requested.

Claims 1, 3, 7, 20, 22, 26 and 39 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 5,488,673 (Katayama) in view of U.S. Patent No. 6,330,075 (Ishikawa), and Claims 4 to 6 and 23 to 25 were rejected under § 103(a) over Katayama in view of Ishikawa and further in view of U.S. Patent No. 6,977,756 (Nakano). Reconsideration and withdrawal of the rejections are respectfully requested.

The claims generally concern an image processing apparatus that quantizes bit-connected image data in a highly efficient manner, ordinarily reducing the required size and complexity of the memory and hardware components of the apparatus. In particular, in the present invention, a bit connection circuit 1, an adder 2 and a latch 3 perform certain processes in response to the decimal portion. This feature converts the data handled by the quantizer 4, the inverse quantizer 5, the substracter 6 and the buffer 8 to integer. Therefore, the claimed invention can reduce circuits handling decimal, and dimension of circuits can also be reduced. Generally, the dimension of circuits handling decimal portions is larger than that of the circuits handling the integer portion.

Referring specifically to the claims, amended independent Claim 1 is

directed to an image processing apparatus for quantizing input image data comprising a bit connection component that connects a decimal portion of corrected image data of a preceding pixel output from a latch component, to input image data of a target pixel as lower bits of the image data of the target pixel, and outputs the bit-connected image data of the target pixel, wherein the bit-connected image data has an integer portion of the image data of the target pixel and the decimal portion of image data of the preceding pixel, a correction component that generates corrected image data of the target pixel by adding a correction value to the bit-connected image data of the target pixel, the latch component that latches a decimal portion of the corrected image data of the target pixel to be connected to image data of a next pixel, without latching an integer portion of the corrected image data of the target pixel, a quantization component that receives an integer portion of the corrected image data without receiving the decimal portion of the corrected image data of the target pixel, and quantizes the received integer portion of the corrected image data of the target pixel, an inverse quantizing component that inverse-quantizes the quantized integer portion of the corrected image data of the target pixel, and outputs an inverse-quantized data of the target pixel, a calculation component that outputs a quantization error of the target pixel based on a difference between the integer portion of the corrected image data of the target pixel and the inverse-quantized data of the target pixel, a buffer that stores the calculated quantization error, and an error diffusion component that generates a correction value by diffusing the quantization error stored in said buffer, wherein the correction value to be added to the bit-connected image data of the target pixel in said correction component is generated by said error diffusion component based on the

calculated quantization errors of neighboring pixels of the target pixel stored in said buffer and diffusion coefficients being smaller than 1.0.

Claims 20 and 39 are method and computer medium claims, respectively, that substantially correspond to Claim 1.

The applied art, alone or in any permissible combination, is not seen to disclose or to suggest the features of Claims 1, 20 and 39, and in particular, is not seen to disclose or to suggest at least the features of i) a latch component (step) that latches a decimal portion of the corrected image data of the target pixel to be connected to image data of a next pixel, without latching an integer portion of the corrected image data of the target pixel, or ii) a quantization component (step) that receives an integer portion of the corrected image data without receiving the decimal portion of the corrected image data of the target pixel, and quantizes the received integer portion of the corrected image data of the target pixel.

Katayama is seen to disclose, referring specifically to Fig. 25, an error-to-be distributed computing means 904 and error distributing means to diffuse error brought from an integer conversion (see, column 20, lines 37-56). The arithmetic-error computing means 905 and the arithmetic-error distributing means add the error to a certain pixel (column 20, line 57 to column 21, line 30). That is, in Kayayama, the integer conversion is done when errors to be diffused to neighboring pixels is calculated from error data arising after a quantization. Katayama points out that this facilitates calculation of the errors to be diffused. Moreover, Katayama points out that the capacity required for a memory for storing the errors to be diffused can be reduced. However, the quantizer (binarizing means) of Katayama must handle must handle the decimal while that of the claimed

invention can handle the integer. Thus, the dimension of the circuit shown in Katayama must be larger than that of the claimed invention.

Additionally, with regard to the latch component, Katayama must perform a certain operation described in column 20, lines 66 to calculate the error (F_D) brought from the integer conversion. This is one of the differences between the claimed invention and Katayama, which comes from the difference of location of the integer conversion between the claimed invention and Katayama.

In addition, as was previously discussed, the reason why a decimal portion occurs is that the diffusion coefficients is smaller than 1.0. Thus, the output being applied with the diffusion coefficients becomes integer and decimal portions. According to the claims, the decimal portion of the integer and decimal portions is split off in front of the quantization component. Therefore, as claimed, "a quantization component (step) that receives an integer portion of the corrected image data without receiving the decimal portion of the corrected image data of the target pixel, and quantizes the received integer portion of the corrected image data of the target pixel". According to the claims, the buffer maintains the quantization error which does not include the decimal portion so as to reduce the memory capacity requirement of the buffer. The reason why the quantization error is only made from an integer is that the decimal portion of the integer and decimal portions is split off in front of the quantization component. Generally, the split off decimal portion introduces lowering of the calculation accuracy. To improve the calculation accuracy, the decimal portion is added to a next pixel. Thus, the bit-connection component as claimed.

Accordingly, Katayama is not seen to disclose or suggest the features of the claims.

Ishikawa and Nakano have been reviewed, but are not seen to compensate for the above-noted deficiencies of Katayama. Ishikawa merely discloses that an output dot pattern is generated directly from a look up table (LUT). Nakano is merely seen to disclose a structure for a data driven device which includes an error diffusion computing unit having an error holding register and an error data memory. However, neither Ishikawa or Nakano are seen to teach anything that, when combined with Katayama, would have resulted in the features of the claims.

In view of the foregoing amendments and remarks, amended independent Claims 1, 20 and 39, as well as the claims dependent therefrom, are believed to be allowable over the applied art.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

REQUEST FOR INTERVIEW

Applicant respectfully requests to conduct a telephonic interview with the Examiner to discuss the foregoing amendments and remarks in further detail. Accordingly, it is requested that, when the Examiner is ready to take up action on this Amendment, that Applicant's undersigned representative be contacted to schedule an interview.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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